An InP HEMT MMIC LNA with 7.2-dB Gain at 190 GHz

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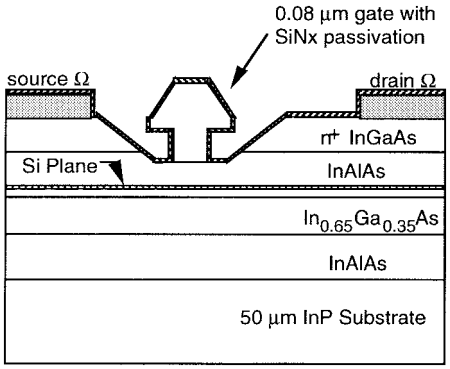
***Abstract*— We present the highest frequency performance of any solid-state monolithic microwave integrated circuit (MMIC) amplifier. A 2-stage 80-nm gate length InGaAs/InAlAs/InP HEMT MMIC balanced amplifier has a measured on-wafer peak gain of 7.2 dB at 190 GHz and greater than 5 dB gain from 170 to 194 GHz. The circuit was fabricated using a pseudomorphic 20-nm $In_{0.65}Ga_{0.35}As$ channel HEMT structure grown on a 3-in InP substrate by MBE. Based on the measured circuit results, the intrinsic exhibits an $F_{\max}$ greater than 400 GHz.**

I. Introduction

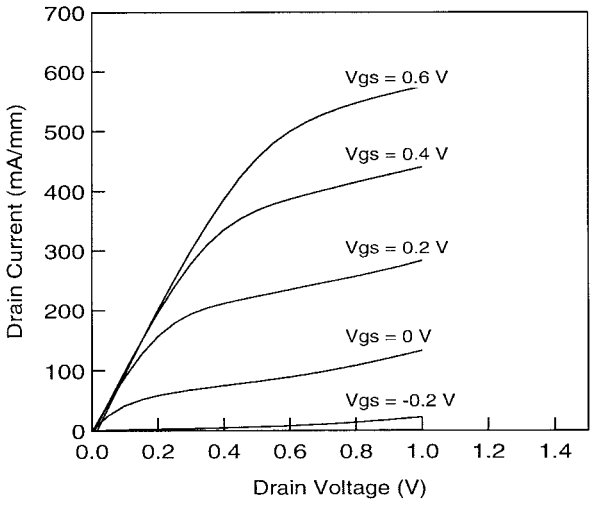
$In_xGa_{1-x}As$/InAlAs/InP high electron mobility transistors (InP HEMT's) have demonstrated the highest extrapolated cutoff frequency (f_T) and maximum oscillation frequency $(F_{\max})$ for a three-terminal device. Cutoff frequencies have been reported in excess of 300 GHz and $F_{\max}$ values have been extrapolated as high as 600 GHz [1]–[3], however devices with high f_T and $F_{\max}$ extrapolated from low-frequency measurements have not directly resulted in demonstrated monolithic microwave integrated circuit (MMIC) amplifiers with gain at frequencies greater than 140 GHz. Recently, we have reported a 3-stage InP HEMT monolithic millimeter-wave integrated circuit low-noise amplifier (MMIC LNA) that demonstrated 12.5 dB gain at 155 GHz [4]. In this letter, we present the first demonstrated 2-stage 190-GHz MMIC LNA that has a measured peak gain of 7.2 dB at 190 GHz. These results demonstrate that high performance InP HEMT amplifiers at 180–200 GHz for atmospheric sensing applications and future advanced communication systems can now be realized.

II. Process Description and Device Results

The MBE grown InGaAs/InAlAs/InP HEMT structure [Fig. 1(a)] was designed with a wide 20-nm 65% Indium composition InGaAs channel on a 3-in InP substrate. The space layer thickness and silicon doping were designed proportionally to accommodate sub-100-nm gate length devices and avoid potential short channel effects. The wafers were fabricated using our 3-in InP HEMT MMIC production process [5] with a gate length of 80 nm and 750-Å silicon nitride passivation. The wafers were thinned to 50-μm substrate thickness and through substrate via holes were wet-etched to provide grounding to the back metal plane. A 50-μm substrate thickness is used to prevent moding effects on the microstrip transmission lines in the 180–200-GHz frequency range. Also, the 50-μm substrate allows the front-side source



(a)



(b)

Fig. 1. (a) Cross-sectional layers of 0.08-μm $In_{0.65}Ga_{0.35}As$/InAlAs/InP HEMT device grown by molecular beam epitaxy. (b) DC I–V curve of 0.08-μm $In_{0.65}Ga_{0.35}As$/InAlAs/InP HEMT device demonstrating high transconductance, low output conductance, and good pinchoff characteristics.

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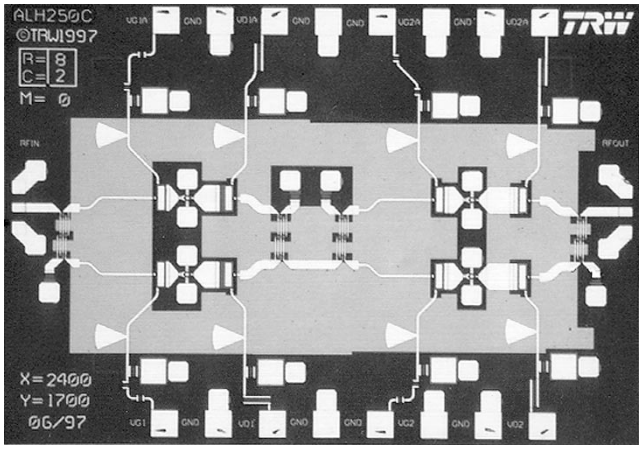

Fig. 2. Photograph of fabricated 2-stage InP HEMT MMIC LNA.

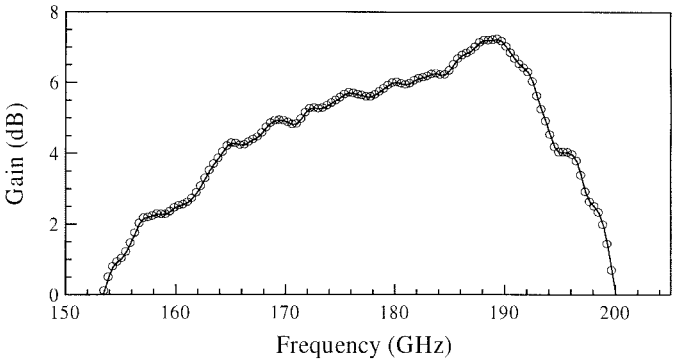

Fig. 3. On-wafer measured gain versus frequency for 2-stage 190-GHz InP HEMT MMIC LNA (bias at $V_d = 1.4$ V, 25 mA).

TABLE I
STATE-OF-THE-ART TRW InP HEMT MMIC HIGH-FREQUENCY LNA'S

Freq. (GHz)	LNA Description	NF (dB)	Gain (dB)	D.C. Power (mW)
94	3-stage LNA	2.9	18	21
118	3-stage LNA	to be measured	18	47
140	2-stage LNA	5.8	9	21
155	3-stage LNA	5.1	10	35
190	2-stage LNA	to be measured	7.2	35
220*	2-stage LNA		6.0*	

*projected data

via pad to be reduced to 80 μm diameter, which lowers the source inductance by greater than 25% compared to the same via on a 75-μm-thick substrate.

Fig. 1(b) shows a typical dc I–V curve of the 80-nm InP HEMT, which exhibits excellent pinchoff characteristics and relatively low device output conductance (Gds). These devices also exhibited an f_T in excess of 250 GHz, a peak transconductance ($G_{\rm mp}$) at 1 V greater than 1000 mS/mm, and a two-terminal reverse breakdown greater than 2 V. The 80-nm gate length HEMT devices exhibited greater than 95% yield for the fabricated wafers.

III. MMIC Design Description and Results

A photograph of the 2-stage 190-GHz LNA is shown in Fig. 2. This amplifier is a two-stage balanced design with a pair of two-finger 30-μm devices in each stage. The size of the chip is 2.4 mm $\times$ 1.7 mm. The small signal device model for this design was scaled based on estimated effects of gate length reduction on gate-to-source capacitance ($C_{\rm gs}$) and gate-to-drain capacitance ($C_{\rm dg}$), source inductance via (L_s), and gate resistance (R_g). No changes were made to $G_{\rm mp}$ and $G_{\rm ds}$ as the thinner spacer and lower doping were designed to avoid short channel effects. The bias networks employed radial stubs for radio frequency (RF) bypass and low-frequency stability R-C networks were added after the radial stubs. The passive elements were carefully analyzed by Sonnet EM analysis software, which is extremely crucial for these ultrahigh-frequency designs. This device model was validated by the first pass success of the circuit design and no oscillations were detected in either the subsequent dc or RF measurements.

The chip was tested on-wafer across a 140–220-GHz bandwidth [6]. Initial correlation and verification of the on-wafer test set with fixtured amplifier data was established on another 180-GHz MMIC chip fabricated on this same wafer run [7]. The 2-stage amplifier exhibits a peak gain of 7.2 dB at 190 GHz and demonstrates greater than 5 dB gain from 170 to 194 GHz with a very low dc power consumption of 35 mW ($V_d = 1.4$ V and $I_d = 25$ mA) as shown in Fig. 3. The measured peak gain of the amplifier matches the simulated gain, although the frequency response was shifted slightly higher by 5%.

IV. Discussion

Table I shows a table of TRW's state-of-art InP HEMT MMIC amplifiers operating between 94–190 GHz. The new 190-GHz amplifier exhibited 7.2 dB gain or 3.6 dB gain per stage. The design included four sets of Lange couplers which contribute at least 0.5 dB of loss per coupler. After accounting for circuit losses, via source inductance and gain mismatch, we estimate that the intrinsic InP HEMT in this circuit has a maximum available gain in excess of 6 dB per stage at 190 GHz, and an $F_{\rm max}$ in excess of 400 GHz. We project that a 2-stage 220-GHz amplifier built on this process will exhibit greater than 6-dB gain.

Devices with a 2-finger gate design with the same circuit topology resulted in as much as a 2.5 dB higher gain per stage than a 4-finger device. The difference in the performance is due to lower device capacitance values, $C_{\rm dg}$ and $C_{\rm gs}$ in the 2-finger device. The device capacitances are composed of an intrinsic and extrinsic component, where the extrinsic component is a function of the number of fingers and is lower for the 2-finger device. The 2-finger device exhibits only 7.26 fF $C_{\rm dg}$ and 24 fF $C_{\rm gs}$ while the 4-finger device has 9.66 fF $C_{\rm dg}$ and 26 fF $C_{\rm gs}$.

V. Conclusion

We have described the development of the first 2-stage InP HEMT MMIC LNA operating at 190 GHz with a peak gain of 7.2 dB. This is the highest frequency 3-terminal amplifier demonstrated to date. Based on the results achieved here, we project that MMIC LNA's operating at 220 GHz with 3 dB gain per stage are achievable with InP HEMT technology in the near future.

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